REMARKS

Claims 29, 33-35 remain in this application. Claims 30-32 have been canceled. Claims 29, 33-35 have been amended.

Examiner S. Loke is thanked for having thoroughly examined the present invention.

Following the suggestion of the examiner, a new title has been submitted in the Amendment which is believed to be indicative of the invention to which the claims are directed, and approval is requested, respectfully.

Reference numeral (140) in Fig. 2e is an oxide layer formed by thermal growth, which is now incorporated into page 14, in conformance with Fig. 2e.

Claim 29 has been amended to remove the reference to ONO.

It is believed that with these corrections, the objection to disclosure has been overcome.

The applicants have found some other informalities which have been corrected as shown in replacement paragraphs in the Amendment Section above. It was also discovered that Fig. 1 was incorrectly labeled in the original application. Corrections have been made in both Fig. 1 as well as on pages 3 and 4 of the specification, with no new matter added. The corrections now remove any confusion that may have existed between Fig. 1 and other Figures. The drawing is being submitted for the examiner's approval.

Reconsideration of the rejection of claims 29-35 under 35 USC 103(a) as being unpatentable over Doan, et al., in view of Hsu, et al., is respectfully requested in view of the amendments and for the reasons given below.

The applicants are in agreement with the examiner that Doan, et al., disclose a stacked-gate flash memory. However, it is respectfully submitted that the stacked-gate flash memory of the instant invention differs from that of the primary reference because of the structural differences. Firstly, the referenced memory cells are constructed over field oxides, as differentiated from the trench oxides that the instant invention employs. The structure of a trench is different from field oxides, primarily due to the depth of the trenches.

Claim 29 has been amended to emphasize the depth of the instant trenches. Furthermore, the high-step oxide used in the instant invention is likewise different structurally from a field oxide because of the height that can be formed with a high-step oxide. This aspect has also been incorporated into claim 29 in order to distinguish even further the present invention from the references. Most importantly, the inside walls of the opening that is formed in between the high-step oxide makes it possible to form a floating gate with tall folding surfaces to provide high coupling between the floating gate and the word line over the control gate, as can be seen in Fig. 3e.

It is respectfully suggested that the combination of these various references cannot be combined without reference to the applicants' own invention. None of the applied references address the problem of inadequate coupling ratio of conventional cells. Applicants have claimed their process in detail. The processes of Figs. 2a-2f and 3a-3g (Claims 29-35) are believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is

desirable. We believe that there is no such basis for the combination. We therefore request respectfully that examiner S. Loke reconsider this rejection in view of these arguments and the amendments to the claims and allow claim 29 and claims dependent from claim 29.

Allowance of all claims, as amended, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. the attached page is captioned **"Version with Marking to Show Changes Made."**

It is requested that should the Examiner not find that the Claims Allowable that are now presented, that he call the undersigned Attorney at 845/452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE

The existing title has been replaced with the following title:

A STACKED-GATE FLASH MEMORY CELL WITH FOLDING FLOATING GATE AND INCREASED COUPLING RATIO

IN THE DRAWINGS

One replacement sheet marked in red for corrections for Fig. 1 is submitted for approval. Corrections are made to erroneously labeled reference characters to distinguish them from the labels in the subsequent Figures. No new matter added.

IN THE SPECIFICATION

On page 2, last paragraph has been amended as follows:

Memory devices include electrically erasable and electrically programmable read-only memories (EEPROMs) of flash electrically erasable and electrically programmable read-only memories (flash EEPROMs). Generally, flash EEPROM cells having both functions of electrical programming and erasing may be classified into two categories, namely, a stack-gate structure and a [stacked-gate] split-gate structure, which is not discussed here. A conventional stack-gate type cell is shown in Fig. 1 where,

On page 3, all of page 3, has been amended as follows:

as is well known, tunnel oxide film [(120)](20), a floating gate [(130)](30), an interpoly insulating film [(140)] (40) and a control gate [(150)](50) are sequentially stacked on a silicon substrate [(100)] (10) between a drain region [(113)](13) and a source region [(115)](15) separated by channel region [(117)](17). Substrate [(100)](10) and channel region [(117)](17) are of a first conductivity type, and the first [(113)](13) and second [(115)](15) doped regions are of a second conductivity type that is opposite the first conductivity type.

The programming and erasing of [an] the flash EEPROM shown in Fig. 1 is accomplished electrically and in-circuit by using Fowler-Nordheim (F-N) tunneling, as it is known in the art [mentioned above]. Basically, a sufficiently high voltage is applied to control gate [(150)](50) and drain [(113)](13) while source [(115)](15) is grounded to create a flow of electrons in channel region [(117)](17) in substrate [(100)](10). Some of these electrons gain enough energy to transfer from the substrate to control gate [(150)](50) through thin gate oxide layer [(120)](20) by means of (F-N) tunneling. The tunneling is achieved by raising the voltage level on control gate [(150)](50) to a sufficiently high value of about 12 volts. As the electronic charge builds up on floating gate [(130)](30), the electric field is reduced, which reduces the electron flow. When, finally, the high voltage is removed, floating gate [(130)] (30) remains charged to a value larger than

On page 4, all of page 4, has been amended as follows:

the threshold voltage of a logic high that would turn it on. Thus, even when a logic high is applied to the control gate, the EEPROM remains off. Since tunneling process is

reversible, floating gate [(130)] (30) can be erased by grounding control gate [(150)] (50) and raising the drain voltage, thereby causing the stored charge on the floating gate to flow back to the substrate. Of importance in the tunneling region is the quality and the thinness of the tunneling oxide separating the floating gate from the substrate.

The thicknesses of the various portions of the oxide layers on the stacked-gate [side (between the control gate and the source) and the stacked-side (between the floating gate and the drain) of the] flash memory cell of Fig. 1[b] play an important role in determining such parameters as current consumption, coupling ratio and the memory erase-write speed, especially in an environment where feature sizes in advanced integrated circuits are being scaled down at a rapid rate. In prior art, various methods have been developed to address these parameters. For example, EPROMs having a trench-like coupling capacitors have been disclosed to address the shrinking area of the gate electrodes, and hence the capacitive coupling ratio between the floating gate and control gates on a conventional prior art EPROM.

In US Patent 5,480,821, Chang discloses a method of fabricating source-coupling, stacked-gate, virtual ground

On page 14, 2nd paragraph has been amended as follows:

The active regions are next defined with a photolithographic step and field regions grown, as is well known in the art. A photoresist pattern is normally used to protect all areas on which active devices will later be formed. The nitride layer is then dry etched, and the pad oxide may be etched by means of either a dry-or wet-chemical process. The etching is further carried into the substrate to form the shallow trench (130) that is shown in Fig. 2b. The photoresist layer is next removed by oxygen plasma ashing and then the inside walls of trench (130) is lined with an oxide layer (140) by thermal growth. Subsequently, the trench is filled with isolation oxide (150), thus forming shallow trench isolation (STI) as shown in Fig. 2b. Next, the substrate is subjected to chemical-mechanical polishing (CMP) after which the nitride layer is removed. The removal of nitride layer can be accomplished in a high-density-plasma (HDP) etcher with etch recipe comprising gases O_2, SO_2, CF_4 and He at flow rates between about 10 to 250, 10 to 80, 0 to 50 sccm and 40 to 80 sccm,

respectively. The pad oxide layer (110) underlying nitride layer (120) is also

On page 18, the 1st paragraph has been amended as follows:

which is then reduced to between about 2000 to 6000 Å after chemical-mechanical polishing. [25] Thus, when, at the next step, nitride layer (220) is removed, a deep opening (235) is left behind. Nitride removal is accomplished using phosphoric acid, H_3PO_4. Pad oxide layer (210) underlying nitride layer (220) is also removed preferably by using wet etch, thus leaving openings (235) in between the isolation oxide "caps" (250) that protrude above the STI (230).

IN THE CLAIMS

Claims 29, 33-35 have been amended and claims 30-32 have been cancelled as follows:

29. (AMENDED ONCE) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:

a substrate having a gate oxide layer;

at least two trenches formed to a depth between about 2500 to 5000 Å below the surface of said substrate;

an oxide liner formed over said substrate, including over the inside walls of said two trenches;

a high-step oxide formed within said two trenches over said oxide liner and protruding upward over the surface of said substrate to a height between about 2000 to 6000 Å;

said high-step oxide forming an opening with high walls over the surface of said substrate between said two trenches;

a first polysilicon layer formed conformally inside said opening and over the surface of the substrate between said high walls to form a floating gate having folding surfaces;

an intergate oxide formed over said floating gate having folding surfaces;

a second polysilicon layer formed protruding downward in between said folding surfaces over said intergate oxide layer to form a control gate; and

[a trench with a high-step oxide;

a conformal layer lining the inside walls of said trench;

an opening adjacent to said trench with a high-step oxide;

a first polysilicon layer conformally lining said opening including high-step oxide of said trench to form a floating gate;

an ONO layer covering said substrate including walls of said floating gate lining said opening;

a second polysilicon layer covering said ONO layer to form a control gate; and]

a self-aligned source (SAS) line.

Claim 30, please cancel.

Claim 31, please cancel.

Claim 32, please cancel.

33. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said opening has a width between about 1500 to 5000 Å.

34. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said first conductive layer is polysilicon [layer has] having a thickness between about 100 to 500 Å.

35. (AMENDED ONCE) The stacked-gate flash memory cell of 29, wherein said second conductive layer is polysilicon [layer has] having a thickness between about 1000 to 3000 Å.